

AMENDMENTS TO THE SPECIFICATION

Amend the paragraph found from page 1, line 28 to page 2, line 7 as follows:

The capture circuit 3 includes a frame buffer memory 31 for storing a frame of video data, and a memory controller 32 for controlling the writing and reading of data to and from the frame buffer memory 31. The capture circuit 3 also includes a data transfer interface 33 for transferring the ~~frame~~ frame of video data read out of the frame buffer memory 31 to the digital broadcast receiver system chip 1 through an external bus 4.

Amend the paragraph found on page 16, lines 5-25 as follows:

As described above, according to the embodiment, the format conversion circuit 100 converts the format of video data VD to the pseudo MPEG2-TS format. Therefore, when the format-converted MPEG2-TS data MD is input to the digital broadcast receiver system chip 1, through the MPEG2-TS input port, the demultiplexer 18 processes the input MPEG2-TS data MD in the same manner as it processes normal MPEG2-TS data. As a result, the captured video data VD can be transferred to the system memory 2 without going through the capture circuit 3 required in the conventional systems. Further, the format conversion circuit 100 is synchronized with the sampling clock CK for the video data VD to write and read the video data into and from the FIFO memory 101, and output the sampling clock CK for the video data VD as it is as the sampling clock CK for the MPEG2-TS data MD. Therefore, the MPEG2-TS data MD can be synchronized with

the video data VD. In addition, the format conversion circuit 100 absorbs, in the horizontal synchronization periods, the delays of processing the video data VD due to the insertion of the packet headers, thereby performing the format conversion in real time.